D0 Muon Scintillator Electronics Front End Module (SFE) Specification

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1. Introduction

Figure 1-1 is a block diagram of the overall Muon Scintillator Front End System consisting of 6500 channels of Photomultiplier Tube (PMT) signals input to approximately 137 Scintillator Front End (SFE) modules, each with 48 channels. The SFE modules are housed in sixteen (16) 9U x 280 mm VME crates located on the D0 Platform and in various places on the detector. Each crate contains a 680xx processor, a Scintillator Readout Controller (SRC) module, a Scintillator LED Pulser (SLP) module and approximately 10 SFE modules. The SFE modules accept and process event data from all crossings and provide an event data buffer for Level 1 accepted events. The SRC collects and further processes Level 1 accepted event data from all SFEs in the crate. The SLP is a test module that is used to stimulate the scintillator counters, producing PMT signals to the SFEs for testing purposes. A summary of SFE specifications is presented in Section 13.

Level 1 (L1) trigger data corresponding to HIT channels is sent directly from each SFE to the Muon Trigger system for each 132 ns crossing interval via a 1 Gbit/s serial link. It is expected that the scintillator system will have a 1% occupancy which implies that on average only one channel will be HIT every other crossing. Event data is processed and temporally stored for each crossing for as long as 4.7 μs while the L1 trigger decision is made. The Muon Trigger system processes the scintillator trigger data along with that of other Muon subsystems and sends its decision to the Trigger Framework (TFW) which processes trigger data from the entire detector. The SRC module receives timing and trigger information about the L1 accepted events from the Trigger Framework via the Serial Command Link (SCL) and passes it on to the SFE modules. Identification of accepted events temporarily being stored in the SFE is determined by the arrival time of an L1 accept signal to within one crossing interval. Upon receipt of the L1 Accept, data from the accepted event is transferred to one of 16 buffer pages of a dual port memory, comprising the SFE L1 Buffer.

Transfer of event data from the SFEs to the SRC is initiated by the SRC immediately following an L1 Accept. The SRC addresses each SFE module in the crate which then outputs its data to one of 16 pages of a dual port memory on the SRC. The dual port on the SRC then serves as an L1 Buffer for the entire crate. After all modules have been read out, the Digital Signal Processor (DSP) on the SRC is notified that the event is ready for readout. The DSP reads, reformats, and transfers

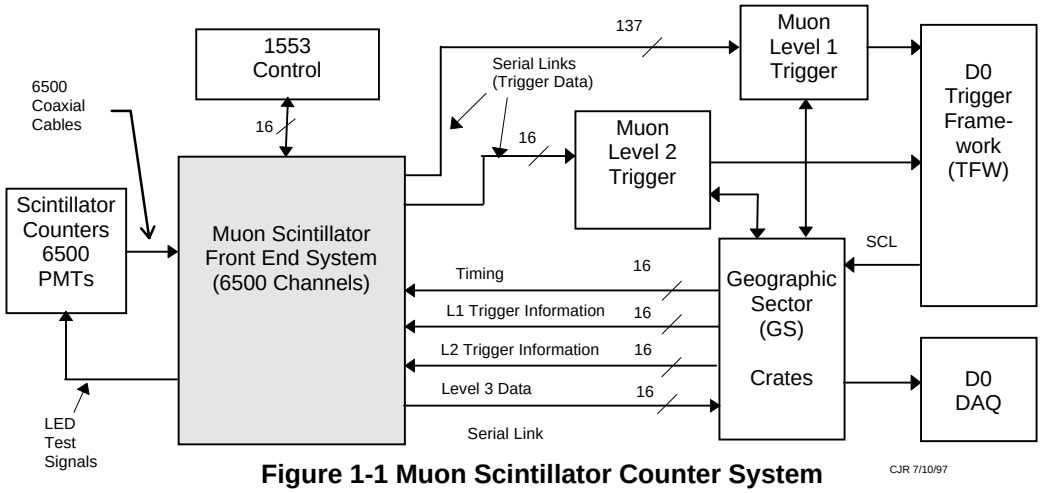

Figure 1-1 Muon Scintillator Counter System

selected event data from the SRC L1 Buffer to a Level 2 (L2) trigger data queue for output to the Muon L2 Trigger System. The DSP awaits the L2 trigger decision from the Trigger Framework and reformats and transfers L2 accepted events to the Level 3 data queue for output to the MRC.

2. General Operational Description

Figure 2-1 is a block diagram of the SFE module whose functions are:

1) Determine if the channel signal was above threshold and its leading edge occurred within the programmable Timing Gate interval of each crossing (i.e. HIT) for the purpose of comprising the L1 trigger data.
2) Measure the relative leading edge timing of each HIT channel to 1 ns resolution for the purpose of comprising the L2 trigger data.
3) Measure the integrated charge input of selected channels during a programmable Analog Gate interval of each crossing for PMT gain monitoring purposes.
4) Generate a front panel Trigger - OR signal for the purpose of generating a local test trigger.
5) Transmit the HIT channel information to the Muon L1 Trigger System for each crossing that is not within the SYNC GAP interval.
6) Store the timing and charge data of each crossing for a programmable period of up to 4.7 μs while an L1 trigger decision is made.
7) Maintain an L1 Buffer for the timing and charge data of up to 16 L1 accepted events.
8) Output the L1 event data to the crate SRC.

Forty-eight PMT input signals are transformer coupled to high speed amplifiers from which two outputs are derived. The first output goes to a two threshold discriminator and the other output goes to one of three 16 channel analog multiplexers. One of three programmable timing gates for each group of sixteen channels along the discriminator outputs are fed to HIT logic which produces the Trigger OR, L1 trigger data, and scintillator input timing signals. Timing measurement of the input signals are made with 4 channel TMC (Time Memory Cell) time digitizer chips developed by Yasuo Arai at KEK National Laboratory for High Energy Physics in Japan. In addition to providing 1 ns timing measurement data, the TMC also contains a dual port memory capable of temporarily storing the timing data for approximately 4.2 μs. An additional 0.5 μs of temporary storage of the timing data is provided in the Delay Buffer (DLY_BUF) logic to make up the required 4.7 μs temporary storage while the L1 trigger decision is made.

The other amplifier output is used measure the integrated charge of the input signal on selected channels. For that purpose, the 48 channels are divided into three groups of 16. Each analog multiplexer selects 1 of 16 channels on a fixed basis or in a rotating mode where the channel selection is incremented at the first crossing interval of each turn. Each multiplexer is followed by an integrator and 10 bit analog to digital converter (ADC). ADC data is delayed in FIFO memories implemented in the Master Control Logic while the L1 trigger decision is made.

The Master Control logic receives the L1 Accept signal from the SRC and provides control signals to each of the 12 Delay Buffers. TMC timing data of the proper event is transferred to the next available input page of a dual port memory called the L1 Timing Data Buffer implemented in each Delay Buffer PLD. A Header Word and three ADC data words are implemented in a dual port memory in the Master Controller called the L1 ADC Data Buffer.

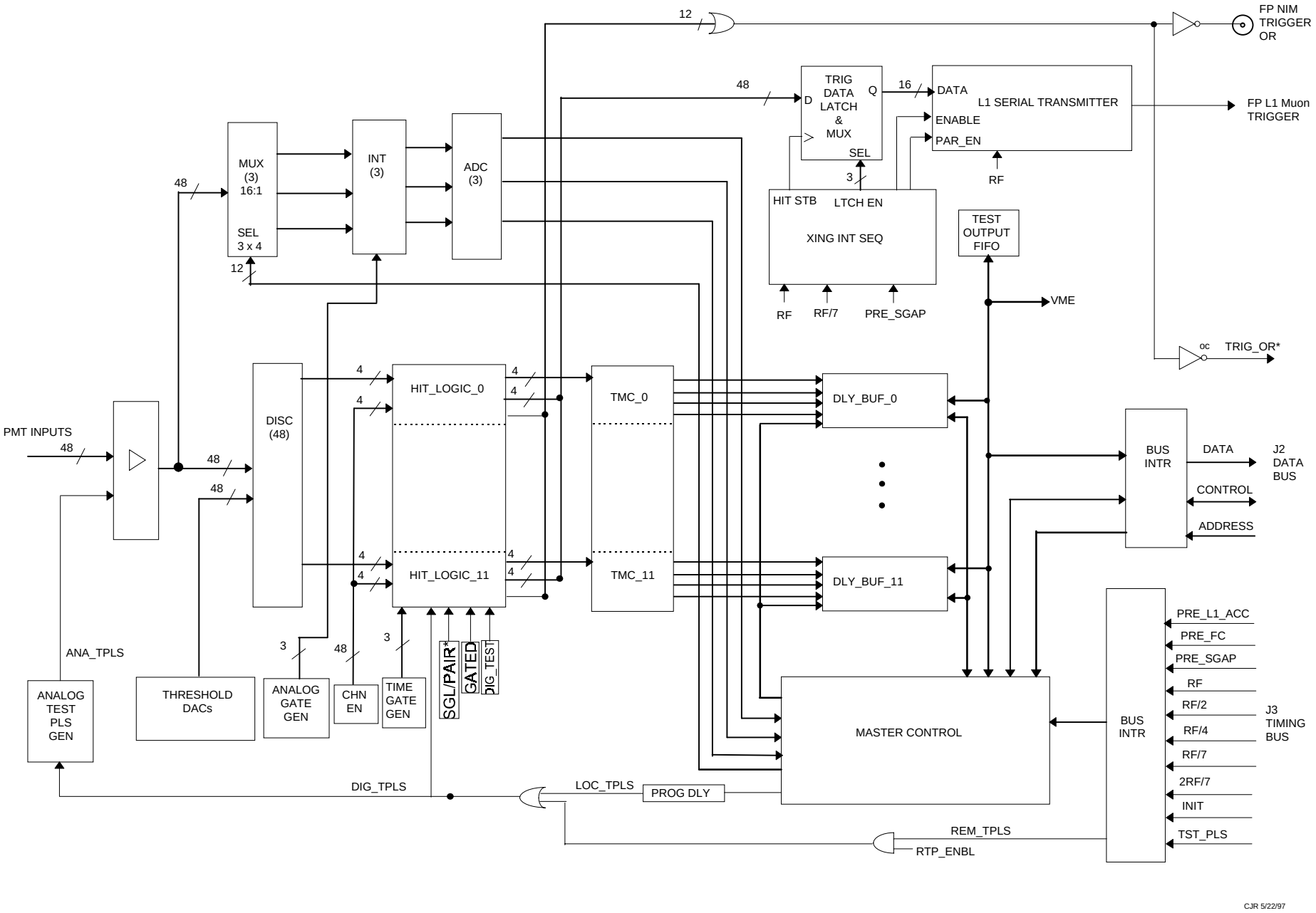

Figure 2-1 Block Diagram of SFE

Readout of event timing and ADC data on each SFE is initiated by the SRC which establishes an address lock with the Master Controller. The Master Controller then outputs the next in order L1 ADC Data Buffer page consisting of a Header Word, containing the SFE board address and the corresponding crossing number of the event, followed by three ADC data words. Each ADC data word consists of the selected group number and corresponding data. These four words are output for every event independent of whether or not any channels were HIT. The Master Controller then broadcasts the L1 Buffer page to be output and a token pulse to all Delay Buffers who respond on one of 12 dedicated lines if any of their four channels are HIT. These dedicated lines are monitored by the Master Controller as well as all other Delay Buffers. Delay Buffer are prioritized by channel number and those having HIT channels output one word consisting of channel number and timing data for each HIT channel. The Master Controller senses that all data has been read out and ends the address lock with the SRC. Readout time estimates for a crate containing 10 SFEs having 1% occupancy are 7.1 μs. The readout time for 100% occupancy is estimated at 47.6 μs.

3. Analog Input Signal Conditioning

3.1. Input Signals Characteristics

Photomultiplier input signals are cabled to the front panel of SFE modules over nearly equal 30 foot lengths of RG58 coaxial cable. The PMT side of the cable has isolated BNC connectors having 100 Ω isolation resistors from the shield to ground. Connections at the SFE are dual Lemo connectors at the front the module.

The input signals are negative going exponentially shaped pulses with a sharp leading edge. Inputs come from two different detector regions whose typical pulse characteristics are:

	Pixel Counter	Central C Layer
rise time (10 - 90)	5 ns	8.5
width @ 50%	11 ns	23 ns
base width @ 10%	29 ns	55 ns
fall time (90 - 10)	21 ns	40 ns
maximum peak amplitude	250 mV	250 mV
minimum peak amplitude	5 mV	5 mV
typical peak amplitude	25 mV	25 mV?

Although the output amplitude of the PMT signals can be controlled by adjusting their high voltage, it is desired that they operate with the lowest possible value to extend the life of the PMTs. The PMT high voltages are adjustable in groups of sixteen. The variance in input signal arrival time on a given module is expected to be 2 - 3 ns. Some of the crates will reside in a magnetic field of approximately 200 gauss.

3.2. Input Amplifier Circuit

Figure 3-1 shows the input amplifier circuit for each channel which is basically the same as that used for the Scintillator Counters in Run I. The shield of adjacent channels are common in the dual Lemo connector and tied to analog ground via a Zero Ω resistor. This resistor will be omitted in the final assembly if experiments show that signal quality is improved by doing so during the prototyping period. The 50 Ω termination of the input cable is through two 25 Ω resistors to ground on the secondary of the isolation transformer which has been tested in magnetic field of up to 300 gauss. A common test pulse will be injected to all channels and is discussed further in Section 7. The NEC 1663 difference amplifier operating at a gain of 10 has a typical bandwidth of 700 MHz. With a ± 5V power supply, the amplifier has a typical output offset of +2.9V and a maximum output swing of 4V p-p. A ± 6V power source derived from ± 12V is used for power in an effort to increase the linear output swing to at least 2.5 V in one direction. Although the amplifier has a differential output, the two outputs are used for different purposes. The negative going output is AC coupled to two MAX 901 comparators with an RC time constant of 100 pf x 1K = 100 ns and is used for timing measurement purposes.

This is chosen to be long enough to preserve the pulse characteristics for timing measurements and short enough to recover the base line between successive pulses (1.32 μs @10% occupancy). The positive going output is AC coupled to an analog multiplexer for charge measurement purposes. The time constant on this output is 1 μs or about 10 times the maximum integration interval. The 33 pf capacitors from the comparator's output to its positive input provides high frequency positive feedback to improve its edge timing behavior.

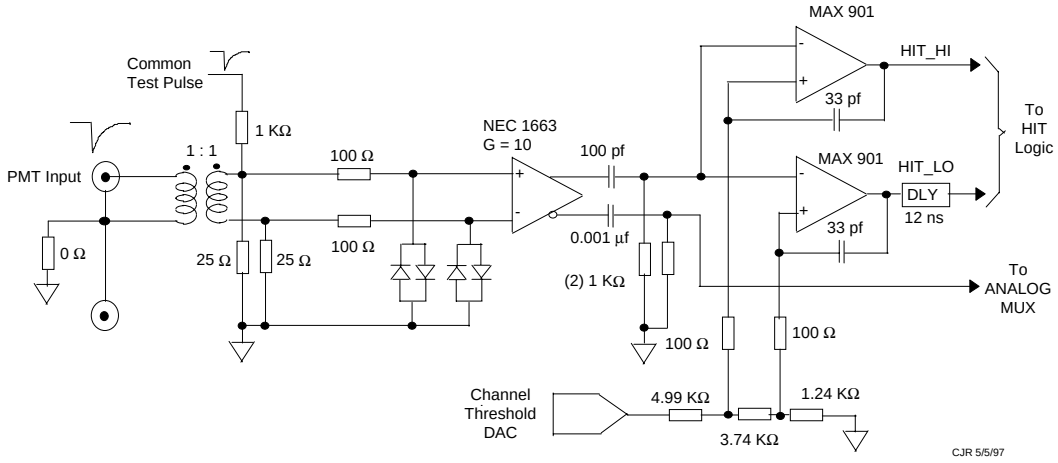

Figure 3-1 Input Amplifier and Discriminator

3.3. Analog Test Pulse Generation

A common analog test pulse is injected into all channels using the circuit in Figure 3-2 where the source is centrally located and drives a 100 Ω micro strip transmission line feeding each channel. An 8 bit DAC is used to set the amplitude and timing is derived from the DIG_TPL generated locally on the SFE or via the backplane by the SRC.

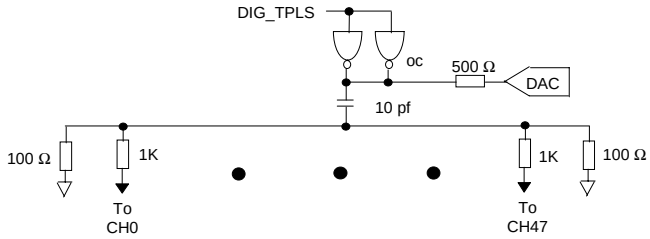

Figure 3-2 Analog Test Pulse Generator

3.4. Discriminator Threshold DACs

The two MAX 901 comparators make up a two level discriminator with the low threshold level fixed at one-fourth of the high threshold level. Each channel has an 8 bit -5V FS output Digital to Analog Converter (DAC) resulting in the following threshold ranges:

	Referred Amplifier Output		Referred to Input	
	1LSB	FS	1 LSB	FS
High Level	-10 mV	-2.55 V	-1 mV	-255 mV
Low Level	-2.5 mV	-638 mV	-0.25 mV	-64 mV

4. Timing Signals Processing

4.1. Timing Gate Generation

A programmable timing gate pulse is generated within every 132 ns crossing interval which is used to limit the processing of discriminator outputs to those only occurring during the gate period. Three timing gates are generated with each going to the HIT Logic of 16 channels. Figure 4-1 shows the logic used to generate the timing gate for which both the delay and width of the pulse are programmable. A 2 bit coarse delay setting along with the RF and RF/7 clocks are input to an Altera Programmable Logic Device (PLD) The logic produces a trigger pulse at one of 4 RF clock edges of the 7 RF periods during each crossing interval. This trigger is input to a 4 bit hybrid programmable delay (DLY 1) having a 2 ns resolution and a maximum delay of 39 ns including a zero step of 9 ns. Because the variable delay range of 30 ns overlaps an RF period of 18.8 ns, two different coarse and fine settings can provide same delay. The output of DLY 1 is input to an RS flip-flop initiating the leading edge of timing gate, TGATE* and to the input of a second programmable delay (DLY2) which controls the width of TGATE*. DLY 2 is a 6 bit device having a 2 ns resolution and maximum delay of 140 ns including a zero step of 14 ns. An erroneous timing gate can be produced if a large width setting causes the timing gate to fall over into the next crossing interval. Should this occur, TGATE_ERR will be latched in a Control and Status Register for diagnostic purposes, but will not effect the SFE operation. The present design has no hardware constraints to prevent this error condition nor is it intended to pass on the error status to the data acquisition system. Note that the TGATE* and TGATE_ERR flip- flops will be implemented inside the Crossing Interval Sequencer PLD.

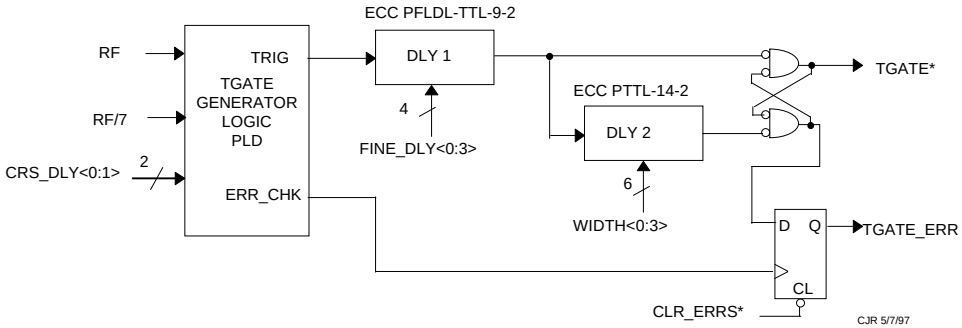

Figure 4-1 Timing Gate Generator

The timing diagram in Figure 4-2 shows the TGATE* timing for both minimum and maximum coarse delay settings and the possibility of overlapping into the next crossing interval. The estimated fine delay range [15..47] and width range [20..145] that are indicated includes logic elements propagation delays in addition to the programmable delays. A summary of the timing gate design parameters are listed below. Delay ranges indicated are relative to RF/7 whose relative phase to the input signals is controlled by the SRC in each crate to a resolution of 1 RF period.

	DELAY	WIDTH
Coarse resolution	18.84 ns	n/a
Fine resolution	2 ns	2 ns
Accuracy @ 25 °C	±1.2 ns	±2 ns
Minimum	±5 ns	20 ns

Maximum	105 ±5 ns	145 ns
Temperature stability (0 -70°C)	-300 PPM/°C	-300 PPM/°
Power supply variation ±5%	-/+ 1.5%	-/+ 1.5%

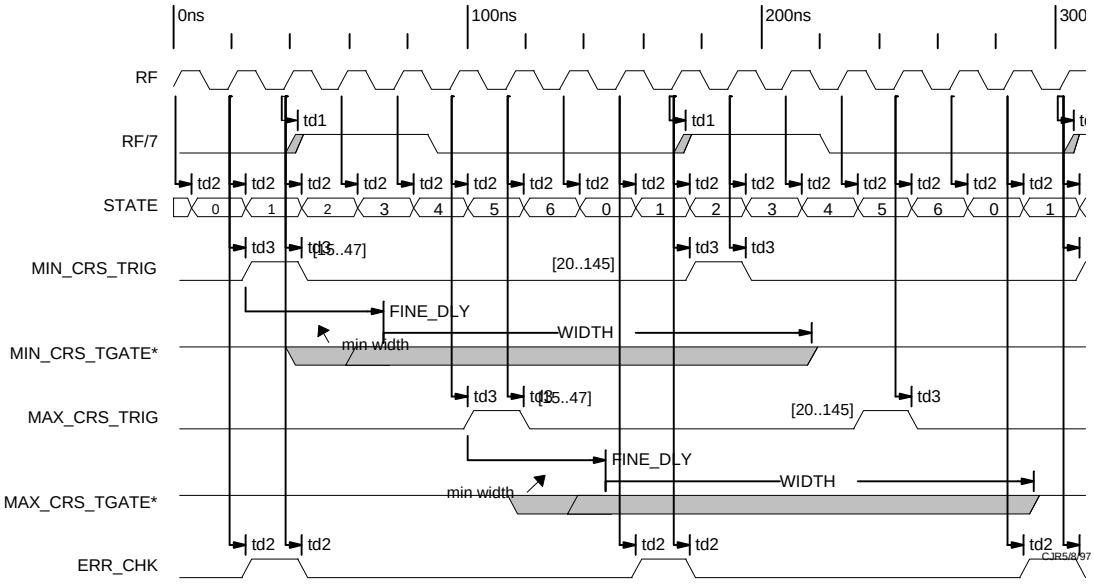

Figure 4-2 Gate Generator Timing

4.2. HIT Logic

Two of the four channels of HIT logic implemented in an Altera 7032 PLD and shown in Figure 4-3. Hit logic I/O include:

Per Channel Inputs

- HIT_HI — HIT_HI output of the discriminator
- HIT_LO_DLY — Delayed HIT_LO output of the discriminator
- EN — Channel enable

Per Channel Outputs

- TMC — Timing signal output to TMC wire-ORed with TST_TMC
- TST_TMC — Test timing signal output to TMC wire-ORed with TMC
- L1SER — Logic output to L1 Serial Link logic

Common Inputs

- TGATE* — Timing gate input
- DIG_TPLS — Digital test pulse timing input
- DIG_TEST — Logic input enables selects DIG_TPLS as timing input.
- GATED — Logic input requires TGATE* for TRIG_OR output
- SGL/PAIR* — When high, TRIG_OR output generated by any HIT channel. When low, TRIG_OR output generated only if both channels of any channel pair are HIT.

Common Output

- TRG_OR — Trigger OR output for the 4 Channels

HIT_LO_DLY is the HIT_LO discriminator output delayed by fixed amount chosen to exceed the maximum rise time of the signal input. Although a HIT on a given channel requires the

coincidence of HIT_HI and HIT_LO_DLY, the timing information is determined by the HIT_LO_DLY input.

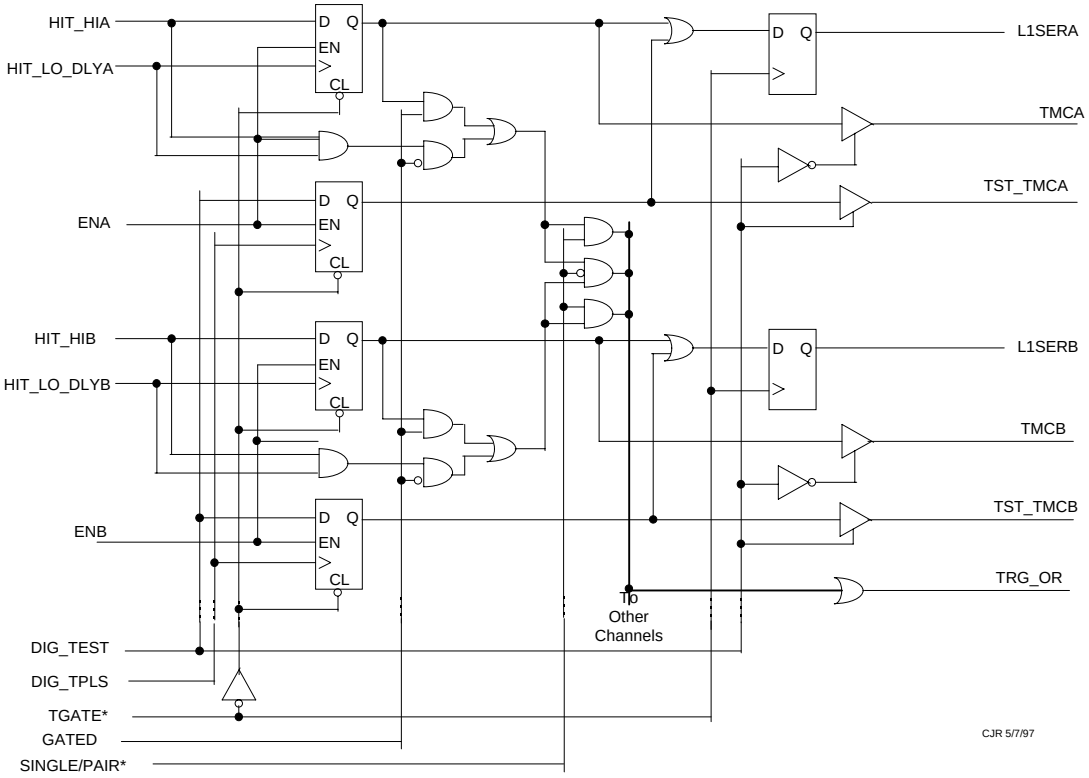

Figure 4-3 HIT Logic of Two Channels

4.3. Output to Muon L1 Trigger

The Output to the Muon L1 Trigger is via a high speed (1 GHz) serial link. Implementation on the SFE uses the Serial Transmitter Daughter Board described in Ref 1. The daughter card mounted on the SFE has a coaxial cable output to coaxial bulk head connector accessible from the front of the module. The trigger data consisting of 48 bits of HIT channel data are latched into three 16 bit latches at the end of each crossing interval. Using the RF clock as a data strobe, this data is input to the serial transmitter during the first 3 of 7 RF cycles in the next crossing interval. The ENABLE input to the daughter board corresponds to the deasserted state of SYNC_GAP and is derived from clocking the inverted PRE_SGAP signal using the RF/7 clock. Another input to the daughter board is PAR_EN (Pairity_Enable) and is generated at the 7th RF cycle of each crossing interval. Figure 4-4 shows the timing signals produced by the L1 Trigger Logic implemented in the Crossing Interval Sequencer PLD. The setup and hold specification of the daughter board are 8 ns and 2 ns, respectively. In the event this is too difficult to achieve, the RF clock to the daughter board can be slightly delayed.

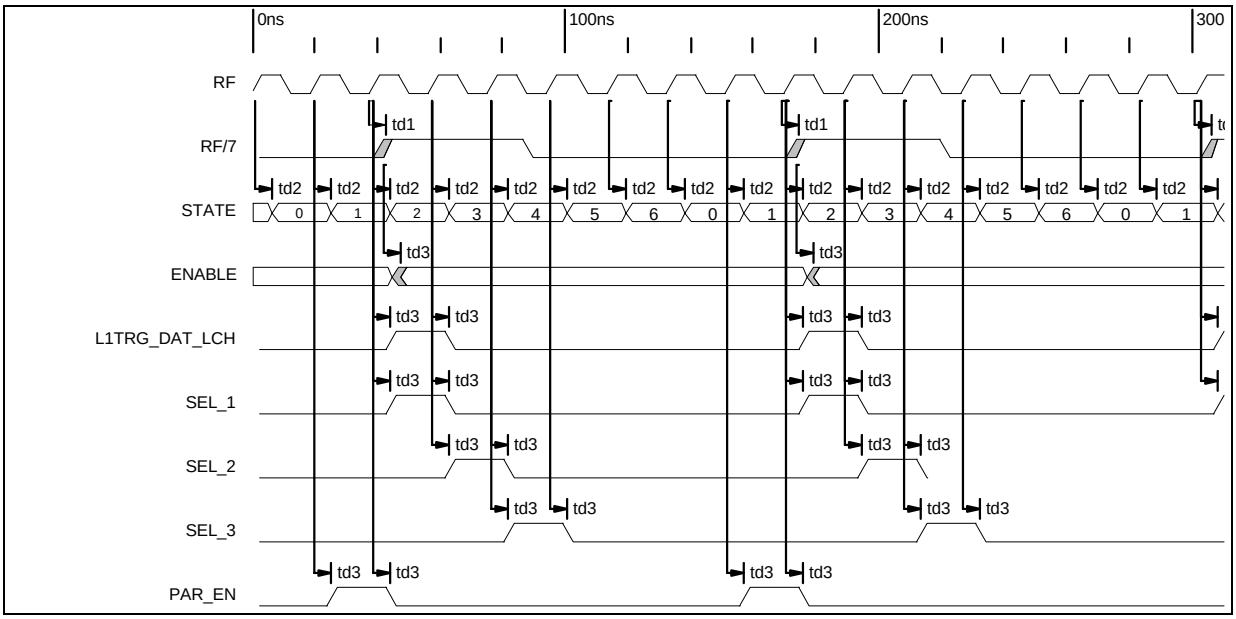

Figure 4-4 L1 Serial Interface Logic Timing

4.4. Trigger-OR Output

The Trigger-OR output of the HIT Logic is the logical sum of HITs on enabled channels. Two independent control modes that are common to all SFE channels further determine the nature of the output. In Gated Mode, only HITs that occur during the TGATE* interval are summed whereas, in Transparent Mode, HITs can occur at any time. In Single Mode, each channel is independent, whereas is Paired Mode, two adjacent channels must both have HITs. The TRG_OR output of each of the 12 HIT Logic PLDs is summed, converted to a Nim level and output at the front panel via a Lemo connector. In addition, the sum is also inverted and output to the backplane using an open collector driver. This bussed Wire-OR signal is used locally by the SRC to generate the L1 Accept after issuing a test pulse. With the Remote Test Pulse enabled, channel HITs can result from test pulses generated on the SFE. When the Remote Test Pulse is disabled and the Scintillator LED Pulser (SLP) module is enabled, HIT channels can result from PMT input signals that resulted from LED flasher inputs to the scintillator counters.

4.5. TMC Time Digitizer

Timing measurements of the input signals are accomplished with twelve 4 channel custom TMCTEG3 time digitizer chips. The TMC is a complex device that has many functions and several modes of operation that are described in Ref 2. However, only those operations that are used by the SFE are discussed here. Although the TMC is run with RF/7 as the clock input, timing measurements are made relative to an internal PLL clock of 4RF/7 (30.3 MHz). Time resolution is determine by dividing each 4RF/7 period (33 ns) by 32 resulting in timing resolution measurement of 1.03 ns.

The leading edge timing of the TMC output of the HIT Logic represents the PMT input or the common analog test pulse times to be measured, whereas the TST_TMC output represents the timing of the common digital test pulse. Each channel's TMC and TST_TMC signals are wire ORed and input to the TMC. Because these signals are latched in the HIT Logic, only one leading edge can occur during a crossing interval. The TMC produces a HIT bit plus 5 bits of timing data corresponding to the arrival time of the leading edge of the input during any of the 4 PLL clock periods of the crossing interval. The output of a separate 2 bit coarse time counter driven at the same rate as the PLL clock is appended to the 5 bits of TMC, providing a continuous 1 ns resolution over the entire crossing interval.

4.6. L1 Trigger Latency Timing Data Storage

In addition to the time digitizer section, the TMC contains a 6 bit by 128 location dual port memory for each channel. The TMC timing data is written to the dual port configured as a FIFO on each PLL clock cycle which also increments both its read and write pointers. By initializing the read and write pointers with a given offset, the dual port performs as a programmable depth FIFO. With 128 locations, the dual port can hold the TMC data for a period of 128 x 33 ns = 4.2 μs. Because the L1 Trigger latency can be larger then 4.2 μs, an additional delay is implemented in the form of a 6 bit wide by 16 bit deep Shift Register adding another 16 x 33 ns = 528 ns for a total trigger latency delay of 4.73 μs. Depth programmability of the overall delay will be via the initial offset of the TMC's read and write pointers.

Figure 4-5 is a functional schematic of the twelve Delay Buffer PLDs and shows each channel's shift register accepting data from its corresponding TMC channel (RX<0:5>). The shift register is clocked by the TMC's write strobe output (WS*) which runs at the 30.3 MHz PLL clock rate. Two bits of common coarse time (CT<0:1>) are produced in the Master Control PLD and input to each Delay Buffer. The 6 bit output of the shift register plus 2 bits of coarse time are clocked into a holding latch by WS*. The common HIT_EN input to the Delay Buffer is also produced in the Master Control PLD and goes high during the crossing interval after the receipt of the L1 Accept signal (PRE_L1ACC). The HIT_EN is combined with the HIT bit output of the timing data holding latch to disable further clocking of the latch. As a result, the coarse time and TMC data corresponding to the first rising edge during a crossing interval is captured in the holding latch awaiting transfer to the L1 Timing Data Buffer.

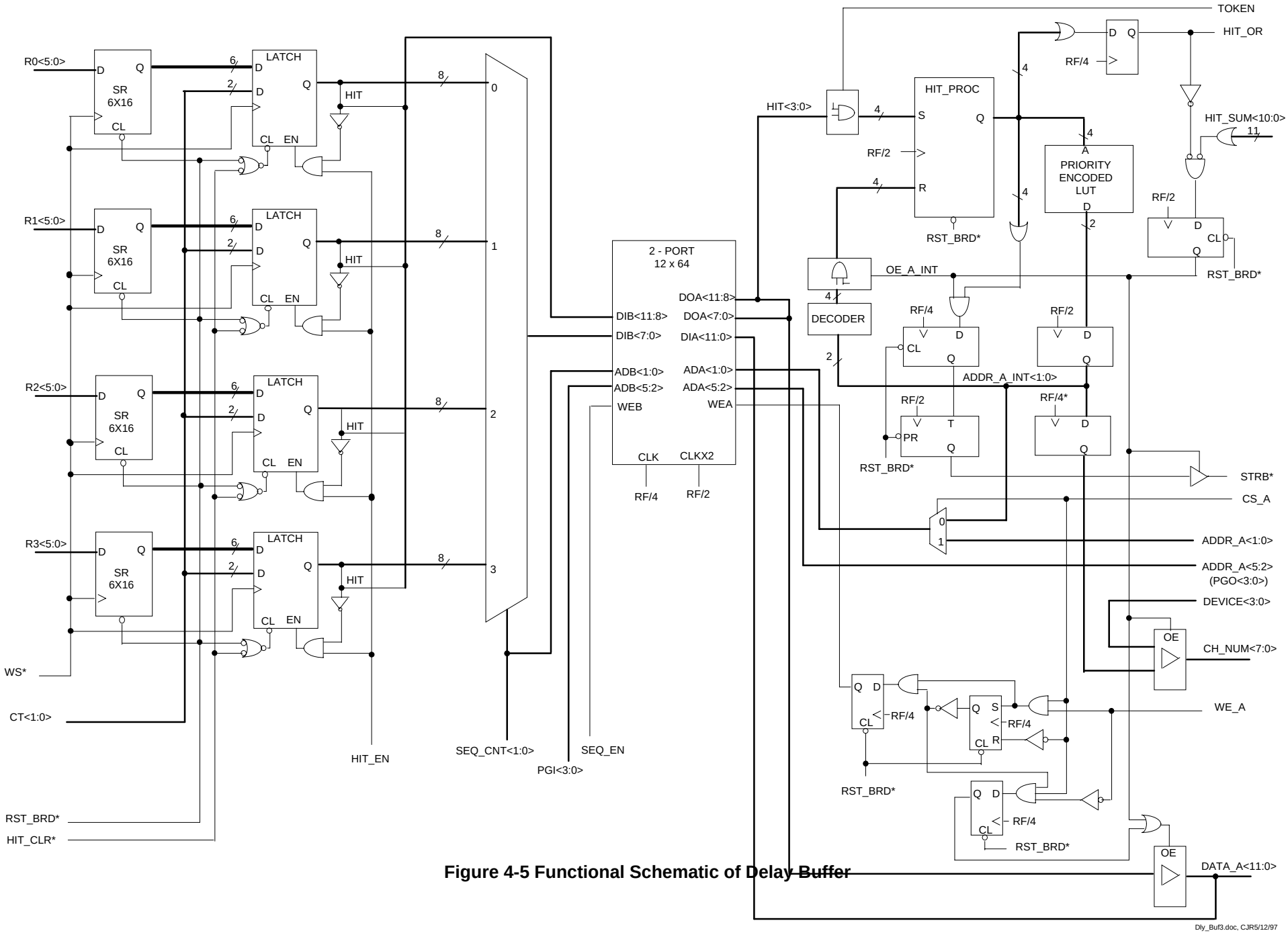

Figure 4-5 Functional Schematic of Delay Buffer

4.7. L1 Timing Data Buffering

The L1 Timing Data Buffer is implemented in a 12 bit by 64 location dual port memory configured within the Delay Buffer shown in Figure 4-5. The dual port is divided into 16 pages of 4 locations, where each location contains the TMC timing data of one channel. The latched TMC data in the holding latch is input to the dual port via the 4:1 MUX in the four RF/4 (13 MHz) cycles following the L1 Accept. This is followed by the HIT_CLR* signal clearing the data in the holding latch making it ready to accept the next event. Although another event could be accepted after 4 crossing intervals or 528 ns, the minimum time between L1 Accepts is expected to be 2.6 μs. PGI<3:0> is a counter used to determine the input page and is incremented after the event data has been stored in the dual port memory. All of the control signals used to transfer the data to the dual port memory are generated in the Master Control PLD and distributed to each Delay Buffer.

5. Analog Signal Processing

The analog signal processing consists of measuring the integrated charge input from selected channels for the purpose of monitoring PMT gain variations over time. The 48 channels are divided into three groups of 16 to allow three channels to be monitored at any given time. The positive going output of the input amplifier circuit shown Figure 3-1 goes to one of three analog multiplexers that select 1 of 16 channels to be monitored. Each multiplexer is followed by an integrator and 10 bit analog to digital converter (ADC). ADC data is delayed in FIFO memories implemented in the Master Control Logic while the L1 trigger decision is made. A 16 page dual port is also implemented in the Master Control PLD and serves as the L1 ADC Data Buffer

5.1. Analog Gate Generation

Three analog gates (AGATE) are generated for use by a corresponding group of 16 channels. It is intended to implement the three analog gates in the same manner with the same specifications as timing gate generators described Section 4.1.

5.2. Analog Multiplexer Channel Selection

Channel selection of each multiplexer is determined by a 4 bit counter output from the Master Control PLD which runs in either a fixed channel mode or in a rotating channel mode. In fixed mode, channel selection is downloaded in VME and the counter is updated at the trailing edge of the FIRST CROSSING interval. In rotating mode channel selection is incremented in a rotating manner at trailing edge of the FIRST CROSSING interval. FIRST CROSSING is used for this purpose to allow for settling time because it occurs in the SYNC GAP when no events are to be accepted.

5.3. Gated Integrator

The gated charge integrator circuit shown in Figure 5-1 is based upon a similar circuit used in Run I and is discussed in Ref 3. Integrator gain is determined the 510 Ω input resistor and the 50 pf integrating capacitor. It is anticipated that values for these components will be selected empirically for best performance. Gain will be determined by Central C Layer signals characteristics such that they yield a +1V full scale output corresponding to the full scale range of the ADC. The AD712 low frequency integrator provides feedback to maintain a zero baseline. The gating interval for each group of 16 channels is determined by a corresponding analog gate signal, AGATE. The integrator reset signal, RST_INT, is common to all 3 integrators and is produced at the end of each crossing interval. RST_INT is implemented in the Gate Generator PLD and is firmware programmable to two RF periods or 38 ns.

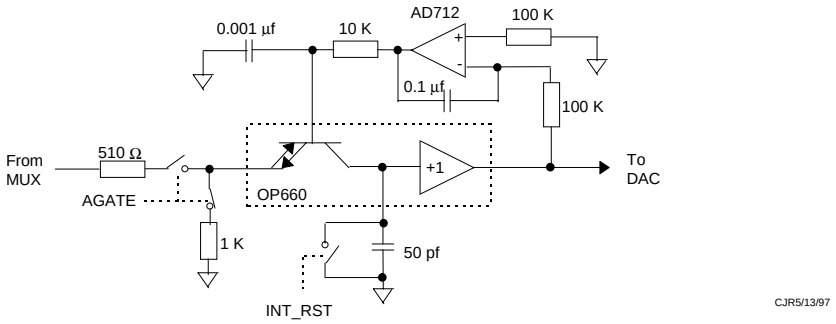

Figure 5-1 Gated Integrator

5.4. Analog to Digital Converter

The AD876 is a 10 bit 20 MSPS ADC that has an on chip sample and hold. The device uses a multistage architecture where the conversion takes place over 3.5 clock cycles (see Figure 5-2) which makes up part of the L1 trigger latency analog data storage. The nominal input range of the ADC is +2 V to +4 V. Hence, the integrator output is amplified by a factor of two and offset by two volts to match the input range of the ADC using an AD818 Op Amp. Reference inputs to the ADC are provided by AD826 Op Amps with an AD586 reference voltage source. OP Amps with high speed and high drive capability were selected to drive the ADC signal and reference inputs to minimize settling time due high capacitive loading by the ADC. Figure 5-2 shows the crossing interval timing signals that are generated for analog signal processing. RST_INT is used in place of ERR-CHK in Figure 4-1 to latch a corresponding analog gate error condition.

5.5. L1 Trigger Latency Analog Data Storage

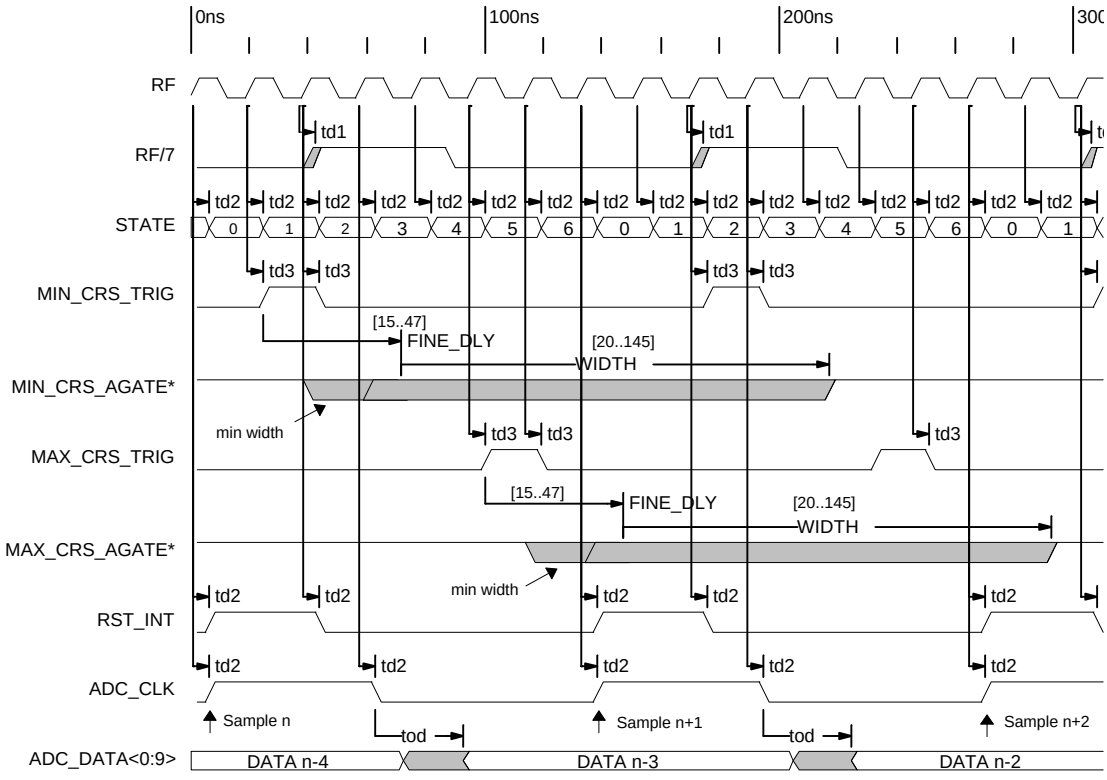

Figure 5-2 Analog Crossing Interval Timing

A programmable depth FIFO implemented in the Master Control PLD plus the 4 stage pipeline architecture of the ADC is used to store the analog data while the L1 trigger decision is made. A 30 bit wide ADC Delay FIFO delays the data from all three ADCs and is shown in Figure 6-3 which along with Figure 6-4 represent a functional schematic of the Master Control PLD. Figure 6-4 contains the VME interface to download several control parameters, one of which is ADC_DEL<5:0> that is used to program the depth of the FIFO. The maximum total delay including the ADC pipeline is (63+4)*132 ns = 8.8 μs.

The Master Control PLD contains a crossing counter (XING_CNT) that is preset (if needed) at the FIRST CROSSING of each turn. The crossing counter is preset to such that it lags the real time crossing number by the value of the trigger latency in crossing intervals. For example if the L1 trigger latency was 35 crossing intervals x 132 ns = 4.6 μs , the crossing counter would be preset to 160 - 35 = 125. When the L1 Accept is received, the crossing counter, XING<7:0>, equals the event crossing number.

In fixed channel mode, the three ADC group channel numbers are input to the Master Control PLD from VME and loaded into the corresponding counter (CHAN_X_CNT) at the interval following FIRST CROSSING. In rotating channel mode the counter is incremented on each at FIRST CROSSING. The counter value is latched by CHAND_X<3:0> when XING<7:0> = 1 and directly output to the analog MUX. This latched value then changes at the same time that the corresponding ADC data is output from the ADC Delay FIFO. If the crossing corresponded to an accepted event, both ADC data and channel number would be latched for transfer to the L1 ADC Data Buffer.

5.6. L1 Analog Data Buffering

Figure 6-3 contains the ADC data holding latch and the logic to control the transfer of the ADC data as well as the TMC timing data to their respective dual ports serving as the L1 Timing Data Buffer. The L1 ADC Data Buffer is a 16 bit wide by 64 location dual port divided into 16 buffer pages. The first location of each page contains that event Header Word and the other three locations contain the ADC data. Transfer from the analog data holding latch to the dual port is identical to the timing data transfer discussed in Section 4.7.

6. Data Output Logic

Transfer of event data from the SFEs to the SRC is initiated by the SRC which successively addresses each SFE module in the crate. After an address lock between the SRC and an SFE is established, the SFE outputs its data to the SRC at a 13 MHz (RF/4) rate. Data is transmitted along a bussed J3 backplane using ABT technology TTL drivers. The Master Control PLD and Delay Buffers interact to output the event data. The readout functions of these devices are:

Readout Functions of Master Controller

- Control addressing handshake with SRC
- Output Header Word from 2-Port L1 ADC Buffer to SRC
- Output 3 ADC data words from 2-Port L1 ADC Buffer to SRC
- Output TOKEN to all Delay Buffers
- Monitor HIT_SUM<11:0> (HIT_ORn of all Delay Buffers) to determine when all Delay Buffers have finished outputting their data to the SRC
- Output DONE to SRC and increment output page pointer

Readout Functions of the Delay Buffer

- Upon receipt of TOKEN, assert HIT_ORn if any of its 4 channels have HIT data
- Monitor HIT_SUM <11:0> composed of HIT_ORn of lower order Delay Buffers
- Output TMC Timing data and channel number of HIT channels from L1 Timing Data Buffer
- Deassert HIT_ORn when done

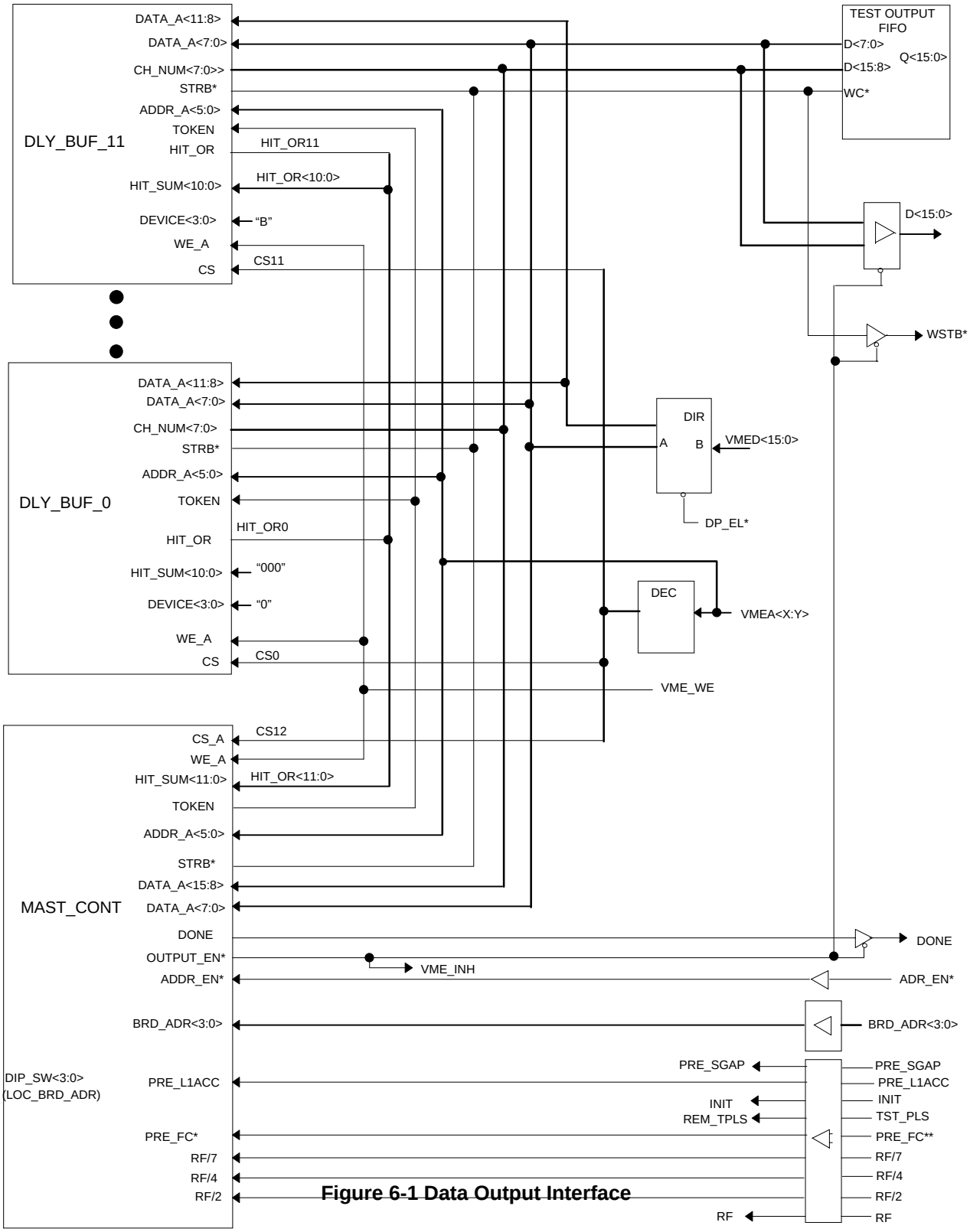

Figure 6-1 Data Output Interface

Although the Header Word and ADC data are output for every event, only timing data of HIT channels are output. The format of the entire event at the SRC is shown Figure 6-2. The First event data word shown is the total word count output of the entire crate and is determined by the SRC. Each word output by the an SFE has a 2 bit Data Type at D<15:14>. Board header words are generated primarily for diagnostic purposes and include the board address (BRD_ADR<3:0>) used by the SRC to address each SFE and the L1_XING<7:0> which is the crossing number of the accepted event.

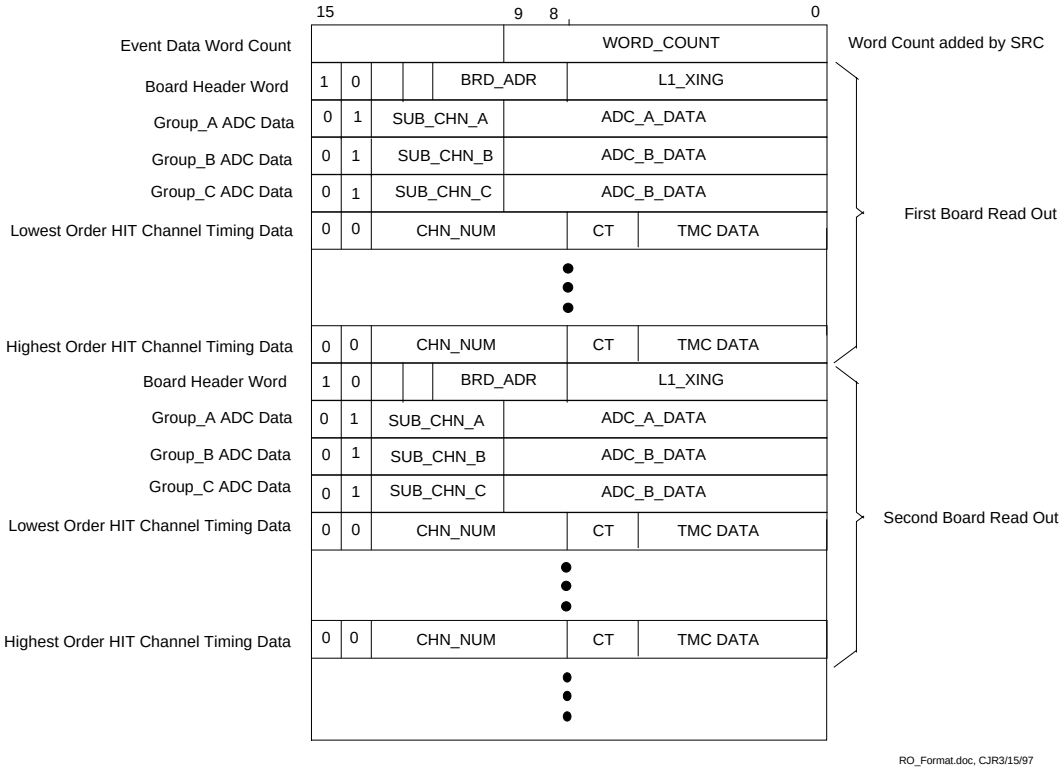

Figure 6-2 Event Readout Format

The readout process begins when the SRC asserts the board address, BRD_ADR<3:0>, along with address enable, ADR_EN. If BRD_ADR matches its dip-switch set board address, the Master Control enables the SFE output drivers by asserting OUT_EN*. The Master Control then output the Header Word followed by the three ADC data words along with a corresponding data strobe, STBB*. The Master Control outputs TOKEN to all Delay Buffers who assert HIT_ORn if they have any channels with HIT data. Delay Buffers are prioritized by board wiring such that the lowest order channels are the first to output their timing data and corresponding 6 bit board channel number. After those Delay Buffers having HIT channels have finished outputting their data, they deassert their HIT_OR. Upon seeing all HIT_ORs deasserted, the Master Control increments the L1 Buffer output page PGO, deasserts OUT_EN* disabling the output drivers, and asserts DONE back to the SRC.

Expected readout times for a crate with 10 SFEs at various occupancies are:

- 1 % Occupancy - 7.1 μs
- 10 % Occupancy - 12.1 μs
- 100 % Occupancy - 47.6 μs

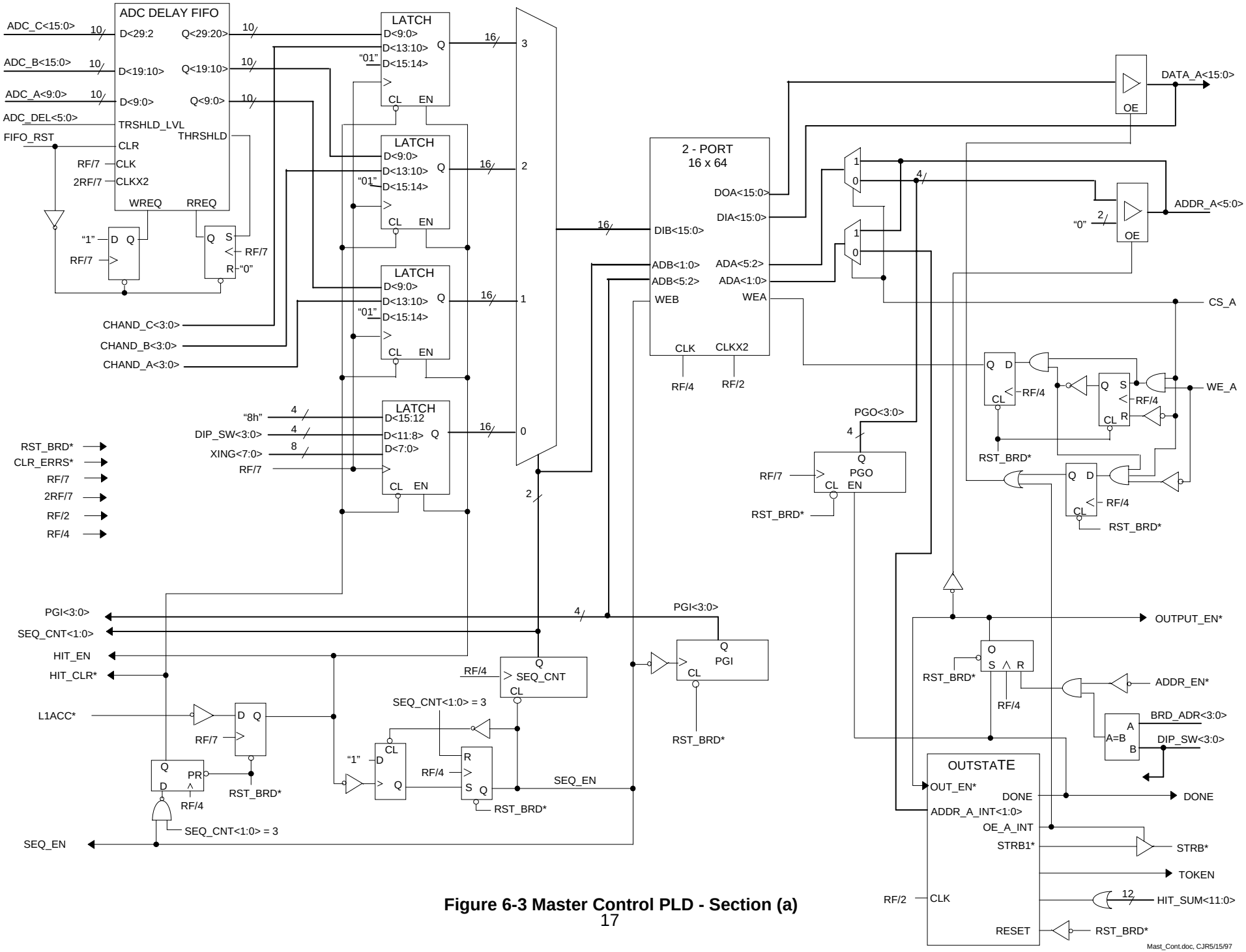

Figure 6-3 Master Control PLD - Section (a)

Mast_Cont.doc, CJR5/15/97

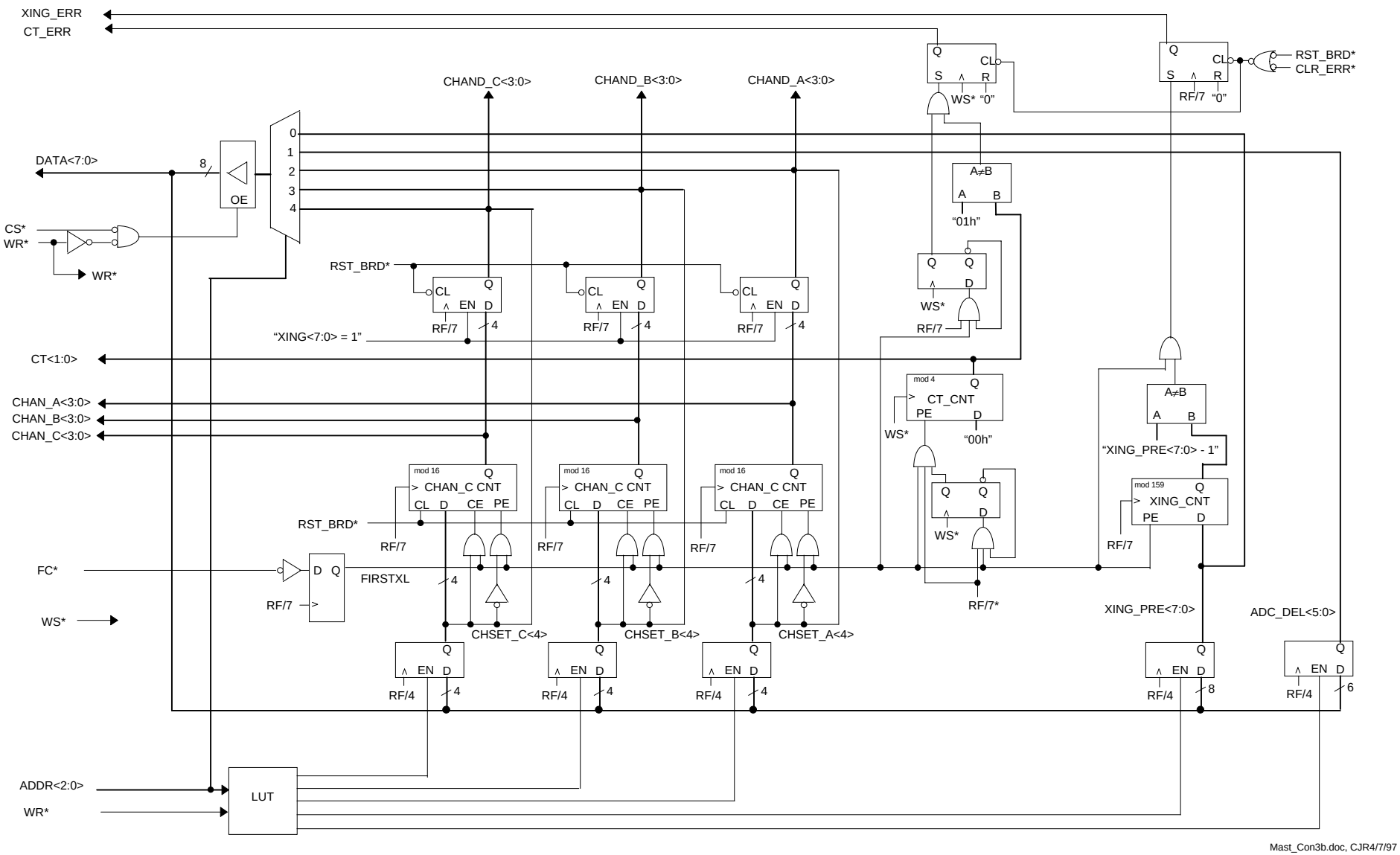

Figure 6-4 Master Control PLD Section b

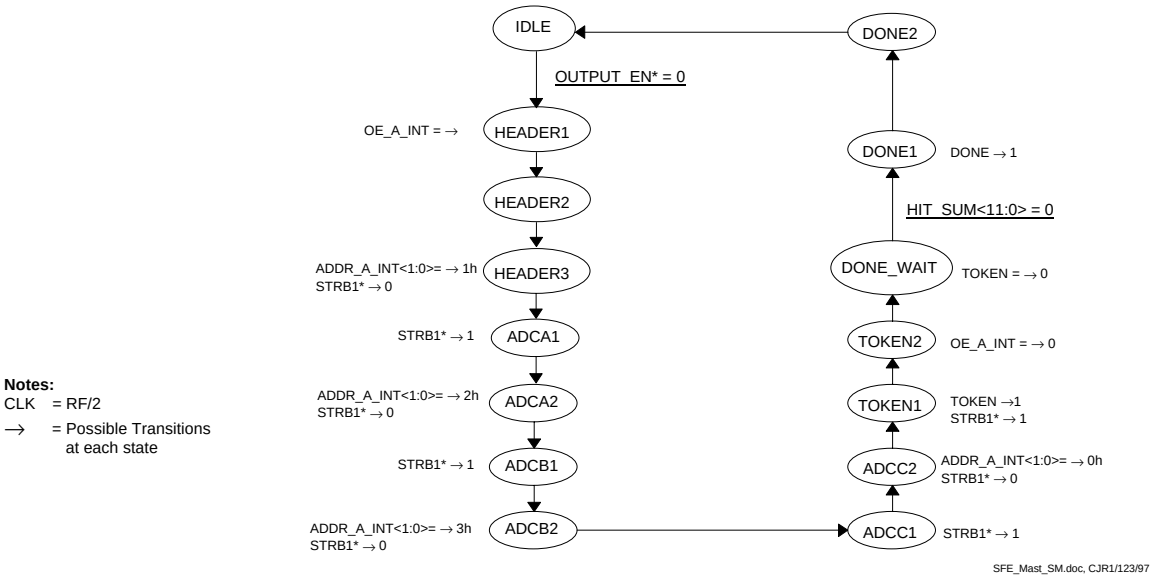

Figure 6-5 Master Control State Machine - OUTSTATE

7. Test Features

In all situations PRE_FC, RF, RF/7, 2RF/7, RF/2, and RF/4 Clocks are supplied by the SRC or a test module.

7.1. L1 Buffer Memory Test

1) Write and Read Test pattern data to L1 Buffer memory via VME

7.2. Circular readout of L1 Buffer

1) Download 16 pages of timing data, ADC data, and header data into respective L1 Buffers (dual ports) of each SFE via each SFE's VME interface.
2) Set SFE to inhibits all writing to dual port from TMCs, ADCs, and Header Latch by disabling all channels.
3) SRC issues PRE_L1ACC or just begins readout. One events worth of data from one or more SFEs are readout by SRC and compared to expected data.
4) Test Output FIFO on each SFE can be read and compared to data read from SRC.
5) Subsequent PRE_L1ACCs read data from consecutive buffer memory pages in a circular manner.
6) Individual SFEs can be tested by initiating a readout under VME control and reading the Test Output FIFO. **(VME issued L1ACC and readout has not been designed)**

7.3. Read TMC test pattern data (This has not been designed)

1) Load all TMC dual ports with test pattern data (i.e. 5's A's 0's 1's) plus HIT bit.
2) Disable data input to all TMC channels of each SFE by disabling all channel.
3) SRC issues PRE_L1ACC. One events worth of data from one or more SFEs are readout by SRC and compared to expected data.
4) Test Output FIFO on each SFE can be read and compared to data read from SRC.

5) Individual SFEs can be tested by issuing L1ACC and initiating a readout under VME control and reading the Test Output FIFO.

7.4. Analog Test Pulse Under SRC Control

1) SRC issued test pulse timing that is programmable with a resolution of 2 ns at any crossing interval in a turn. The test pulse rate is limited by a prescaling the number of turns between test pulses from 1 to 65536 or a minimum rate of less then 1 Hz.
2) SRC issues PRE_L1ACC at appropriate time considering L1 trigger latency.
3) Amplitude of test pulse is controlled by SFE VME.
4) Channel enabling, discriminator threshold levels, and timing gate settings determine what channels are read out.
5) Output to Muon L1 Trigger occurs.
6) SRC reads out event.

7.5. Analog Test Pulse Under SFE VME Control

1) With Digital Test Mode of HIT Logic disabled, one shot local test pulse is generated within any VME programmable crossing interval. Coarse delay resolution of 18.8 ns, and fine delay resolution of 2 ns over a 31 ns.
2) One shot TST_L1ACC generated at VME programmable crossing interval following local test pulse.
3) Amplitude of test pulse is controlled by SFE VME.
4) Pulse amplitude, channel enabling, discriminator threshold levels, and timing gate settings determine what channels are read out.
5) Output to Muon L1 Trigger occurs.
6) Test Output FIFO can be read and compared to expected data.

7.6. Digital Test Pulse Generation Under SFE VME Control

1) With Digital Test Mode of HIT Logic enabled, one shot local test pulse is generated within any VME programmable crossing interval. Coarse delay resolution of 18.8 ns, and fine delay resolution of 2 ns over a 31 ns.
2) One shot TST_L1ACC generated at VME presetable crossing interval following local test pulse.
3) Channel enabling, and timing gate settings determine what channels are read out.
4) Output to Muon L1 Trigger occurs.
5) Test Output FIFO can be read and compared to expected data.

8. Reference Timing Signal and Clock Distribution

Reference Timing signals and various clocks are generated on the SRC and distributed to all SFEs with Low Voltage Differential Signaling (LVDS) technology along flat cable using the a and c rows of J2. One or more grounded wires on the cable bus separate each signal pair for the purpose of reducing signal crosstalk. Bussed timing signals include:

Clock Signals	Frequency
RF	53.1 MHz
RF/2	26.6 MHz
RF/4	13.3 MHz

Timing Signal	Frequency
PRE_FC	47.7 kHz
PRE_SGAP	47.7 kHz
PRE_L1ACC	n/a

RF/7	7.6 MHz	TST_PLS	n/a
2RF/7	15.2 MHz	INIT	n/a

Although INIT is not a timing signal and has no current use in the SFE design, it is carried on this bus because of its relationship to PRE_FC and possible future use. PRE_FC, PRE_SGAP, and PRE_L1ACC all are retimed by RF/7 on the SFE to produce FC, SGAP, and L1ACC, respectively. The SRC adjustment resolution of these timing signals and the RF/7 and 2 RF/7 clocks relative to the beam is 1 RF period over a minimum range of 300 ns. The SFE requires 50 ±5% duty cycle clocks hence, the RF/7 and 2RF/7 clocks are regenerated using a MC88915 PLL clock driver on the SRC.

The cable buss skew across 12 SFE slots is measured at 3.1 μs and timing jitter is less than 1 ns pp. There is no means to compensate for this skew on each SFE.

9. VME Interface

Each crate contains a 680xx processor for parameter downloading, process monitoring, and diagnostic purposes only, it does not participate in the data acquisition process. Because the Scintillator crates are located on the detector and the D0 Platform, remote access to the 680xx is limited to a serial 1553 interface whose transfer rate limited at a single crate to xxbytes/sec. Since there is no direct remote access available for the crates 680xx processor, a remote access interface is implemented with a 1553 interface on the SRC. The 1553 interface interrupts the 680xx which then fetches the download information via the SRC's VME slave interface.

The VME interface is implemented using a non-volatile Alter 7XXX to provide primitive VME functions and an Altera Flex 10K device for address decoding and control logic.

Functions of the VME interface on the SFE include:

1) Control and Status Register bits
   - Reset Board (pulse)
   - Clear Errors (pulse)
   - Reset TMC (pulse)
   - Digital Test Mode (R/W)
   - Trigger OR Gated/Trans* Mode (R/W)
   - Group A Timing Gate Error (R)
   - Group B Timing Gate Error (R)
   - Group C Timing Gate Error (R)
   - Coarse Time Counter Error (R)
   - Output FIFO Empty (Read Only)
   - Remote Test Pulse Enable
   - Reset Output FIFO (pulse)
   - Reset ADC FIFO (pulse)
   - Test Pulse enable (pulse)
   - Configure Flex (pulse)
   - Trigger OR Single/Pair* Chan Mode (R/W)
   - Group A Analog Gate Error (R)
   - Group B Analog Gate Error (R)
   - Group C Analog Gate Error (R)
   - Crossing Counter Error (R)
   - Configure Time Out Error
2) Three Timing Gate Registers (16 bit R/W)
   - 2 bits coarse delay - 18.8 ns resolution
   - 4 bits fine delay - 2ns resolution
   - 6 bits width - 2ns resolution
3) Three Analog Gate Registers (16 bit R/W)
   - 2 bits coarse delay - 18.8 ns resolution
   - 4 bits fine delay - 2ns resolution
   - 6 bits width - 2ns resolution
4) Crossing Number L1 Latency Preset (8 bits R/W)
5) ADC FIFO Delay (6 bit R/W)
6) Three ADC Channel Select (5 bits R/W)

- 4 bits group sub-channel select
- 1 bit enable rotating mode

7) L1 Buffer Page (8 bit Read only)
   - 4 bits Input Buffer page - PGI
   - 4 bits Output Buffer Page - PGO
8) Test Pulse Amplitude (8 bits R/W)
9) Test Pulse Timing (14 bit R/W)
   - 8 bit crossing interval
   - 2 bits Coarse Delay
   - 4 bit Fine Delay
10) Test L1ACC Crossing Number (8 bits R/W)
11) Three channel enable Registers (16 bit R/W)
12) Threshold DAC Control (14 bits R/W)
   - 8 bit DAC setting
   - 6 bit channel select
13) TMC CSR (12 bits R/W)
   - 8 bit data
   - 4 bit TMC select
14) Dual Port Memory of each L1 Timing Data Buffer (12 bit R/W)
15) Dual Port Memory of L1 Analog Data Buffer (16 bit R/W)
16) Output FIFO (16 bit Read only
17) Flex Configuration Memory (8 bit R/W)
18) Configuration Init Done (14 bits Read only)
19) Configuration Status (14 bits Read only)
20) Configuration Ready (14 bits Read only)

10. Front Panel Connectors and Displays

Most of the front panel area is consumed by the 48 board mounted double Lemo input connectors for which no actual front panel is possible. A small area of front panel is provided for LEDs

10.1. Front Panel Connectors

Signal Name	Connector Type	Signal Level
• 48 PMT signal inputs	Lemo	analog pulse
• Trigger OR output	Lemo	Nim
• L1 Serial Link	MCX 50Ω?	Giga Bit Link

10.2. Front Panel Displays

Module Select LED (Yellow)

Power On for each voltage if possible (Green)

11. Power Requirements

The following are very approximate power requirements:

Voltage	Current	Comment
+5V	3 A	
-5V	25 ma	
+6V	700 ma	Derived from +12V

-6V	700 ma	Derived from -12V
+3.3V	1.1 A	Derived from +5V

12. In Circuit Programmability of Programmable Logic Devices

The SFE has Fourteen (14) Altera Flex 10K FPGA type programmable logic devices that require configuration at power up. A non-volatile flash memory holds the configuration files which are automatically downloaded to the Altera 10K devices at power up. The flash memory can be rewritten from VME allowing much of the SFE logic to be in circuit programmable. Several other Altera 7XXX devices including the VME Primitive Interface, HIT Logic PLDs, and Crossing Interval Sequencer PLD will be in circuit programmable whenever reasonably possible.

13. Specification Summary

ANAOLG INPUTS

- 48 channel front panel PMT Lemo inputs
- Negative going signal range : - 5 mV to -250 MV
- Input termination : 50 Ω
- Each channel individually enabled

HIT DISCRIMINATOR

- 2 level threshold discriminator at fixed 4 : 1 ratio
- Individual channel threshold adjustment
- FS high level: -255mV (referred to input)
- High level resolution: -1mV (referred to input)

TIME MEASUREMENTS

- 1.03 ns resolution
- 7 bit binary output over entire 132 ns crossing interval

ANALOG CHARGE MEASUREMENT

- 10 bit ADC
- One channel from each of three groups is monitored on each crossing interval
- Channel Selection is in a Fixed Mode or Rotating Mode

TIMING GATE

- Three individually controllable Gates
- DELAY
  - Coarse Resolution: 18.84 ns (1/RF)
  - Fine resolution: 2 ns
  - Fine adjustment range 31 ns
  - Accuracy @ 25°C: ±1.2 ns
  - Minimum setting: ±5 ns relative to start of crossing interval (RF/7)
  - Maximum setting: 105 ±5 ns relative to start of crossing interval (RF/7)
  - Temperature stability (0-70°C): -300ppm/°C

- Power Supply Variation ±5%: -/+ 1.5%
- WIDTH
  - Resolution: 2 ns
  - Range: 20 ns to 145 ns
  - Accuracy @ 25°C: ±2 ns
  - Temperature stability (0-70°C): -300ppm/°C
  - Power Supply Variation ±5%: -/+ 1.5%
- TGATE ERROR is generated if gate is asserted beyond 113 ns of crossing interval

ANALOG GATE

- Three individually controllable Gates
- DELAY
  - Coarse Resolution: 18.84 ns (1/RF)
  - Fine resolution: 2 ns
  - Fine adjustment range 31 ns
  - Accuracy @ 25°C: ±1.2 ns
  - Minimum setting: ±5 ns relative to start of crossing interval (RF/7)
  - Maximum setting: 105 ±5 ns relative to start of crossing interval (RF/7)
  - Temperature stability (0-70°C): -300ppm/°C
  - Power Supply Variation ±5%: -/+ 1.5%
- WIDTH
  - Resolution: 2 ns
  - Range: 20 ns to 145 ns
  - Accuracy @ 25°C: ±2 ns
  - Temperature stability (0-70°C): -300ppm/°C
  - Power Supply Variation ±5%: -/+ 1.5%
- AGATE ERROR is generated if gate is asserted beyond 94 ns of crossing interval

L1 TRIGGER LATENCY STORAGE RANGE

- Programmable from 4 to 36 crossing intervals (528 ns to 4.75 μs

L1 BUFFER

- 16 events deep

L1 SERIAL LINK OUTPUT

- HIT status of each enabled channel at every crossing interval
- Outputs also generated under test pulse conditions

TRIGGER OR OUTPUT

- Single Channel or Paired channel mode select
- Gated or Transparent mode select

- Nim front panel output
- TTL open collector output to L2 timing bus for SRC generation of L1 Accept under test conditions

TEST PULSE GENERATION

- Remote Analog Test Pulse
  - Test pulse timing derived externally from SRC
  - L1 Accept timing derived from SRC
  - Common channel timing ±0.5 ns
- Local Analog Test Pulse
  - Test pulse timing VME programmable with resolution of 2 ns in any crossing interval
  - L1 Accept timing programmable in any crossing interval
  - Common channel timing ±0.5 ns
- Local Digital Test Pulse
  - Test pulse timing VME programmable with resolution of 2 ns in any crossing interval
  - L1 Accept timing programmable in any crossing interval
  - Common channel timing ±0.5 ns

ERROR STATUS BIT

- Error conditions do not inhibit data acquisition
- TGATE ERROR - Timing gate asserted too close to next crossing interval
- AGATE ERROR - Analog gate asserted too close to next crossing interval
- CT ERROR - Coarse Time Counter Error
- XING ERROR - Crossing Counter Error

DATA OUTPUT

- 13 MHz rate
- Readout time at 1 % occupancy: 7.1 μs
- Readout time at 10 % occupancy: 12.1 μs
- Readout time at 100 % occupancy: 47.6 μs

References

1 Serial Transmitter
2 TMC manual
3.D0 Muon System Upgrade D0Note 2370